AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

1. (Currently Amended) A multi-mode ~~Input/Output (I/O)~~ input/output circuit ~~for transmitting and receiving data between integrated circuits (ICs), wherein each IC contains at least one of said I/O circuits~~, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry configured to send data to another ~~IC~~ integrated circuit, and said receiver circuitry configured to receive data from another ~~IC~~ integrated circuit, said ~~I/O~~ input/output circuit being constructed with ~~CMOS-based~~ complementary metal-oxide-semiconductor based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

2. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry is configured to send data to receiver circuitry in another ~~IC~~ integrated circuit over a first conductor of a pair of adjacently disposed conductors, and where said receiver circuitry is configured to receive data from transmitter circuitry in another ~~IC~~ integrated circuit over a second conductor of the pair of adjacently disposed conductors.

3. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit.

4. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in one of a plurality of double single-ended, ~~CMOS~~

complementary metal-oxide-semiconductor voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of ~~said~~ receiver circuitry in another ~~IC~~ integrated circuit.

5. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in one of said plurality of double single-ended, ~~CMOS~~ complementary metal-oxide-semiconductor voltage level link modes, or in said differential voltage or current mode links, and wherein the ~~ICs~~ integrated circuits at each end of the link may operate with different supply voltages.

6. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a double single-ended voltage mode link mode.

7. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a double single-ended current mode link mode.

8. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

9. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

10. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

11. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by single differential current mode link with a differential input drive.

12. (Currently Amended) ~~A~~ The multi-mode ~~I/O~~ input/output circuit as in claim 1, wherein certain switches are provided to convert said ~~I/O~~ input/output circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

13. (Currently Amended) A method, comprising:

providing at least two integrated circuits ~~(ICs)~~ to each contain at least one input/output ~~(I/O)~~ circuit, said ~~I/O~~ input/output circuit comprising at least one of transmitter circuitry or receiver circuitry, the transmitter circuitry configured to send data to another ~~IC~~ integrated circuit, and the receiver circuitry configured to receive data from ~~IC~~ integrated circuit, the ~~I/O~~ input/output circuit being constructed with ~~CMOS-based~~ complementary metal-oxide-semiconductor based transistors; and

selectively interconnecting together the ~~CMOS-based~~ complementary metal-oxide-semiconductor based transistors with switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

14. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry sends data to receiver circuitry in another ~~IC~~ integrated circuit over a first conductor of a pair of adjacently disposed conductors, and where said receiver circuitry receives data from transmitter circuitry in said another ~~IC~~ integrated circuit over a second conductor of the pair of adjacently disposed conductors.

15. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit.

16. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in one of a plurality of double single-ended, ~~CMOS~~ complementary metal-oxide-semiconductor voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of ~~said~~ receiver circuitry in another ~~IC~~ integrated circuit, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit.

17. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a double single-ended voltage mode link mode.

18. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a double single-ended current mode link mode.

19. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

20. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

21. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

22. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing the switches for operating in a mode defined by single differential current mode link with a differential input drive.

23. (Currently Amended) ~~A~~ The method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing said switches for operating in one of said plurality of double single-ended, ~~CMOS~~ complementary metal-oxide-semiconductor voltage level link modes, or in said differential voltage or current mode links, and wherein the ~~ICs~~ integrated circuits at each end of the link may operate with different supply voltages.

24. (Currently Amended) ~~A~~ The method as in claim 13, wherein certain switches are provided to convert said ~~I/O~~ input/output circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

25-38. (Canceled)

39. (Currently Amended) ~~A device~~ An apparatus comprising:

a plurality of integrated circuits ~~(ICs)~~ and at least one multi-mode Input/Output ~~(I/O)~~ circuit configured to cause the apparatus at least to send and receive data between at least two ~~ICs~~ integrated circuits, where each of the at least two ~~ICs~~ integrated circuits contains

at least one of said ~~I/O~~ input/output circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry configured to send data to another ~~IC~~ integrated circuit, and said receiver circuitry configured to receive data from another ~~IC~~ integrated circuit, said ~~I/O~~ input/output circuit being constructed with ~~CMOS-based~~ complementary metal-oxide-semiconductor based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

40. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry sends data to receiver circuitry in another ~~IC~~ integrated circuit over a first conductor of a pair of adjacently disposed conductors, and where said receiver circuitry receives data from transmitter circuitry in said another ~~IC~~ integrated circuit over a second conductor of the pair of adjacently disposed conductors.

41. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit.

42. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in one of a plurality of double single-ended, ~~CMOS~~ complementary metal-oxide-semiconductor voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of receiver circuitry in another ~~IC~~ integrated circuit.

43. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in one of said plurality of double single-ended, ~~CMOS~~ complementary metal-oxide-semiconductor voltage level link modes, or in said differential voltage or current mode links, and wherein the ~~ICs~~ integrated circuits at each end of the link may operate with different supply voltages.

44. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a double single-ended voltage mode link mode.

45. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a double single-ended current mode link mode.

46. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

47. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

48. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

49. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by opening or closing

switches for operating in a mode defined by single differential current mode link with a differential input drive.

50. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where certain switches are provided to convert said ~~I/O~~ input/output circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

51. (Currently Amended) ~~A device~~ The apparatus as in claim 39, where at least one of said plurality of ~~ICs~~ integrated circuits comprises a radio frequency ~~IC~~ integrated circuit, and where at least one other one of said ~~ICs~~ integrated circuits comprises a baseband ~~IC~~ integrated circuit.

52. (Currently Amended) ~~A~~ The multi-mode input/output circuit according to claim 1, where in the single differential current mode a current drawn from said at least one of transmitter circuitry or receiver circuitry is constant.

53. (Currently Amended) The method ~~according to~~ as in claim 13, where in the single differential current mode a current drawn from said at least one of transmitter circuitry or receiver circuitry is constant.

54. (Currently Amended) ~~A device~~ The apparatus ~~according to~~ as in claim 39, where in the single differential current mode a current drawn from said at least one of transmitter circuitry or receiver circuitry is constant.